

System Level ESD: An ounce of Prevention is Worth a Pound of Cure

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More frequently these days, I have had customer interactions like the one I did recently. It seems a somewhat frantic engineer called our team at Semtech for some 11th hour help in solving his system level ESD problem. Now this fellow had been ambushed by some pretty troublesome ESD spikes. Not only was his product failing in compliance, but he was even seeing ESD induced failures in some early field trials. To make matters worse, he was quickly running out of time to solve these issues. His management was growing impatient, and to add to the pressure there was a big, demanding end customer waiting on this product. The schedule could not tolerate another delay and the situation was growing serious when he reached out to us.

As we talked more with this engineer to understand the challenge and the nature of the problem, it became apparent there were a few simple things that, if applied on the front end of the design cycle, could have helped create a “softer landing” in solving the issues.

First off, our friend had not implemented protection clamps at any of the I/O interfaces of the product. At a minimum, it would have been wise to layout the PCB pads for TVS clamps as a “safety valve” move should he need protection. Even if he did not populate those pads with ESD clamp devices, at least he would have allowed for the option to later do so. However, what really made this product an EMC challenge was the high-speed performance silicon driving the I/O. While the latest (65nm, 45nm and 28nm) high-speed communication ICs offer incredible speed and power saving performance, they also tend to be more susceptible to latch-up or damage from fast rise-time ESD transients. As it was, even a weaker/lower threshold ESD zap could send his board out of commission.

As we talked more, we learned a bit of the history. Without any ESD clamps, the first rev of his board failed ESD compliance miserably. So, in the second revision of the board, our friend implemented a bit better ESD plan. In the second revision he had apparently found and sourced a TVS clamp with an ESD rating to +/-15kV. He sprinkled a few of these at the I/O ports of his board and rather happily assumed that this part bought him a robust +/-15kV ESD immunity for his system. While it was a step in the right direction, there was still a basic misunderstanding of the ESD threat. The rev 2 board spin – back from the board shop and into the compliance lab – still failed well below +/-15kV. Though at this point, with the TVS in the circuit, he did see some modest improvement with the TVS to the system robustness.

Now, with two strikes against him, he turned to us in a panic. And, as we talked through the issues, I really felt this engineer’s angst. In fact, it really seemed that the ESD transients running amok on his PCB traces not only threatened to kill the communication ICs on his board, but this whole situation literally threatened to kill his job. He needed a solution – and fast! So with the clock ticking and the impatient cries of the end customer growing louder, we took over. He sent his boards to our Semtech Protection lab with the objective to safeguard and harden the product from ESD. In essence, if we could deliver a workable solution in short order and do *our job*, we would save his. No pressure!

The first thing that we needed to dispel, however, was the misunderstanding about the system level robustness and the ESD rating of the TVS device. While the ESD rating on the TVS device datasheet pertains to the TVS clamp device, it has very little to do with the system level protection he would achieve on his PCB. That device rating applies to the failure threshold of the TVS device itself but it does not imply the immunity level guaranteed the system. As it was, his system circuit was so sensitive that with the capacitance constraints and size requirements for the TVS part, achieving +/-15kV of system level immunity was going to be extremely challenging.

What's more, we explained that not all TVS devices are constructed the same way or perform in the same basic way. In fact, there can be a wide variation in clamping voltage performance between two TVS clamp devices from different manufacturers. When tight product schedules are on the line, choosing cheap, copycat TVS devices is a bad strategy. In these situations, you need well engineered, proven solutions.

So, we retrofitted his board with some of Semtech's newer, high performance, low clamping devices – devices highly engineered to squash the high peak current. With that, there was marked improvement in the ESD immunity. His system now comfortably passed +/-8kV at this point (for most designs, +/-8kV is sufficient). The board was still not passing +/-15kV contact discharge (a stretch objective), but he was seeing vast improvement from the second revision of his main PCB.

We still wanted to try to push the system immunity higher to meet his stretch objective. So, at this point, we added a small bit of series resistance on the data line – enough resistance to squelch residual transient current, but not significant enough to impact the signal performance. While adding the resistance was not ideal, it did in fact serve to bolster the ESD immunity. And, at such a late stage in the design cycle, the additional series resistance provided a rather easily implementable fix.

In the end, what initially looked like a looming disaster all turned out well: a robust product, a happy-end customer, a pleased boss, and an engineer with a deeper appreciation for system level ESD protection fundamentals. As they say, "an ounce of prevention is worth a pound of cure". And, I would guess that on his next design our friend will be a lot more proactive in planning on the front end of his design to avoid any 11th hour EMC miscues. Perhaps he will even call us again, though hopefully much earlier in the design cycle.